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| UNIVERSITY OF INFORMATION TECHNOLOGY  **COMPUTER ENGINEERING DEPARTMENT** | **MID-TERM EXAMINATION II (2018-2019)**  **COURSE: DEGITAL LOGIC DESIGN**  *Time duration: 90 minutes*  *(Paper materials are allowed)* |

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| **STUDENT NAME: ……………………………………ID: …………..ORDER:…** |

# Question 1 (3 points)

Design 1M x 8 RAM using 256K x 1 RAM chips

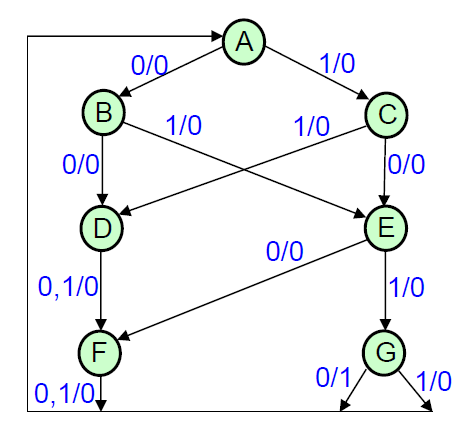
# Question 2 (3 points)

Derive the minimal-state FSM from the state/output table shown in below table:

|  |  |  |  |
| --- | --- | --- | --- |
| **Present**  **state** | **Next state** | | **Output**  **Z** |
| **W = 0** | **W = 1** |
| A | B | C | 1 |
| B | D | F | 1 |
| C | F | E | 0 |
| D | B | G | 1 |
| E | F | C | 0 |
| F | E | D | 0 |
| G | F | G | 0 |

# Question 3 (4 points)

For the state diagram shown in below figure, derive the state encoding using the prioritized-adjacency heuristic:



**This examination’s learning outcomes (LO) (matching to subject syllabus’s LO)**

|  |  |  |
| --- | --- | --- |
| **Question** | **LO** | **Description** |
| 1 | G1.2 | **Be able to design the data path** |
| 2 | G1.1 | **Be able to analyze the finite state machine** |
| 3 | G3 | **Be able to read the reference books** |

**Approved by Head of Subject Designed by**

**Lâm Đức Khải Lâm Đức Khải**